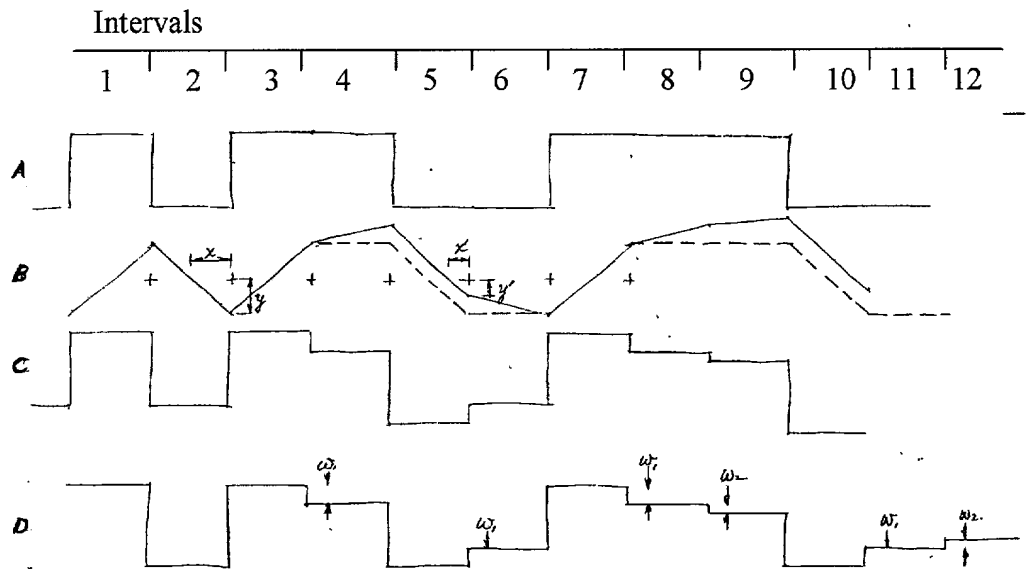

Fig. 1

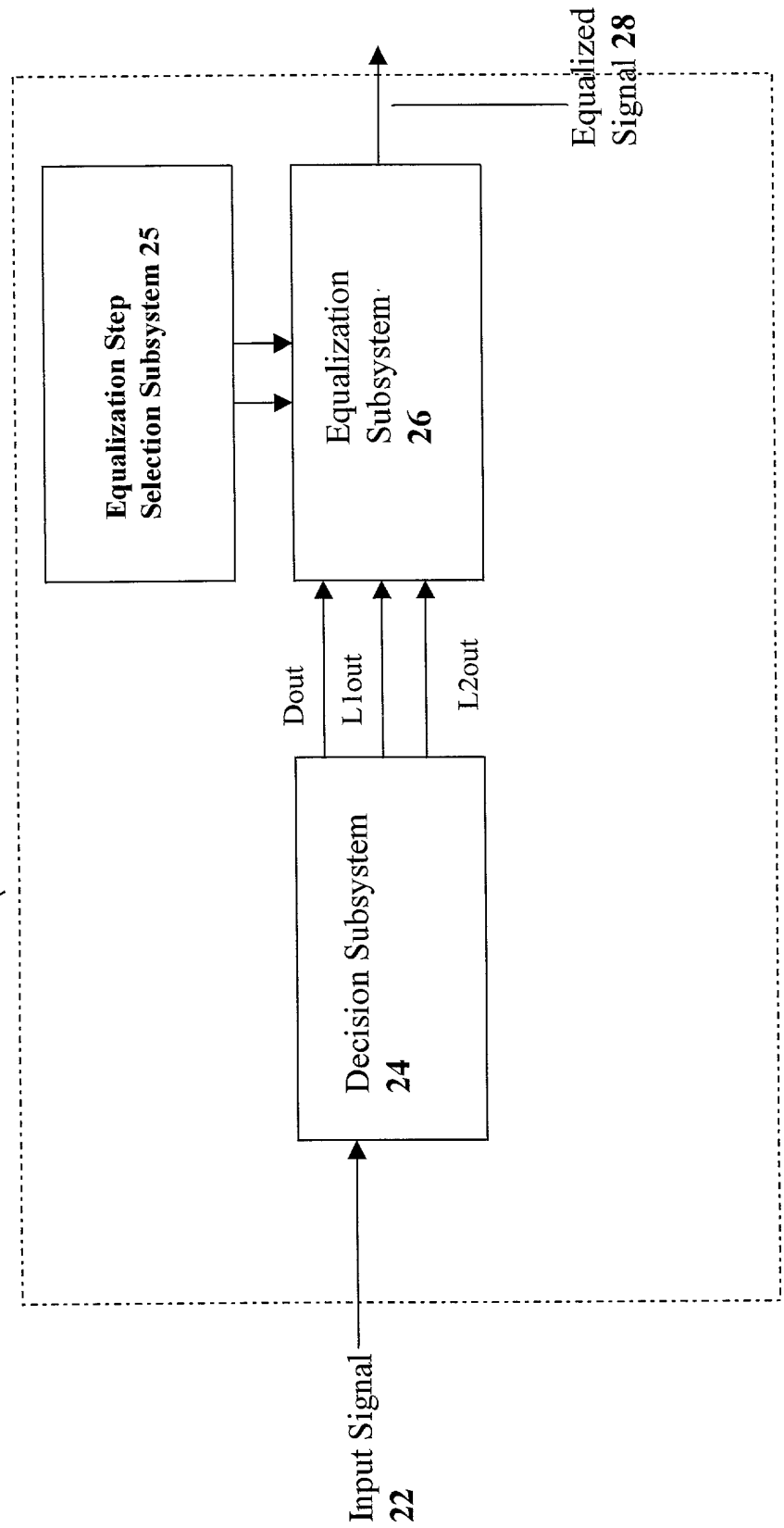
EQUALIZATION SYSTEM 20
Input Signal 22
Decision Subsystem 24
Dout
L1out
L2out
Equalization Step Selection Subsystem 25
Equalization Subsystem 26
Equalized Signal 28

Fig. 2

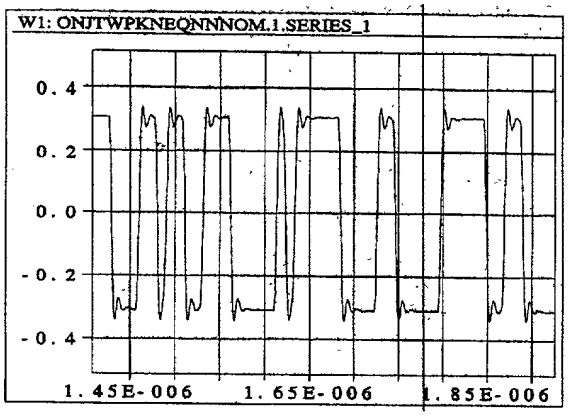

Fig. 3(a)

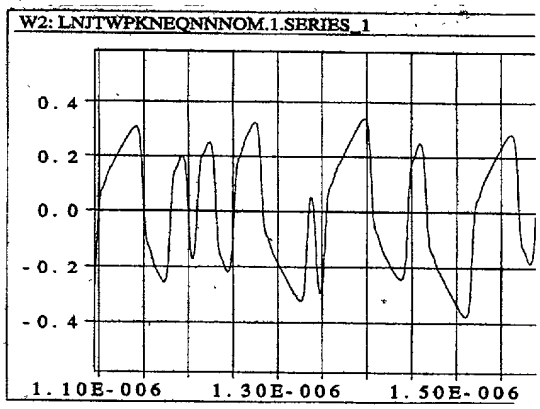

Fig. 3(b)

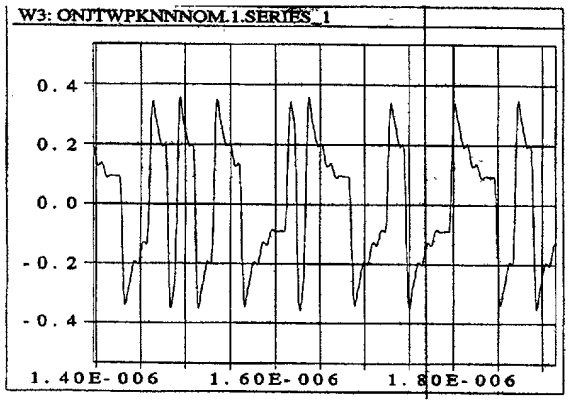

Fig. 4(a)

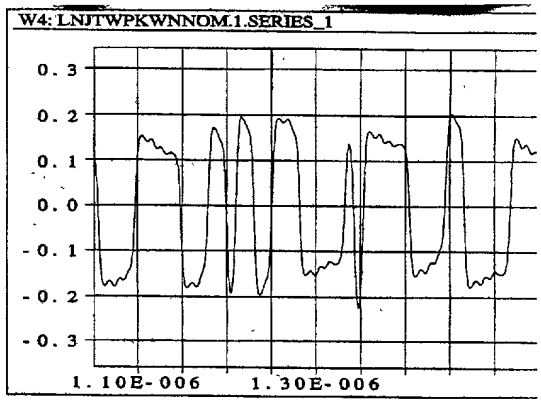

Fig. 4(b)

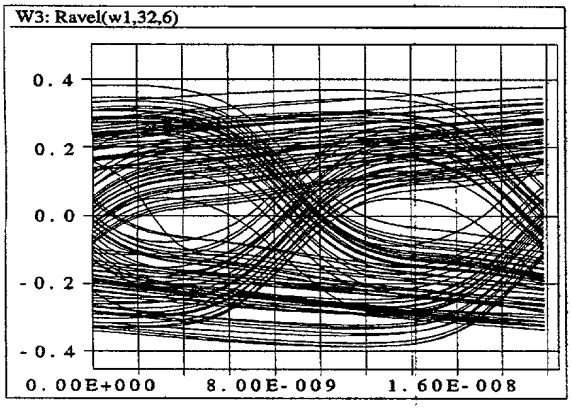
W3: Ravel(w1,32,6)
0.4
0.2
0.0
-0.2
-0.4
0.00E+000
8.00E-009
1.60E-008

Fig. 5(a)

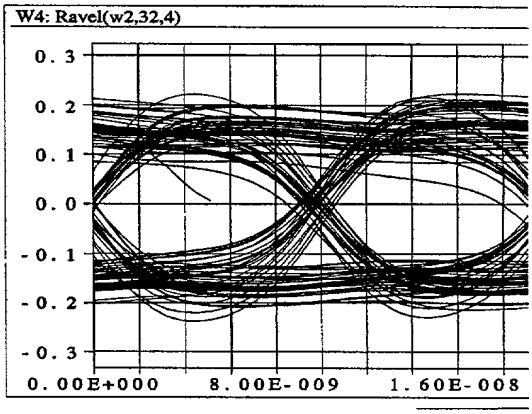
W4: Ravel(w2,32,4)
0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
0.00E+000
8.00E-009
1.60E-008

Fig. 5(b)

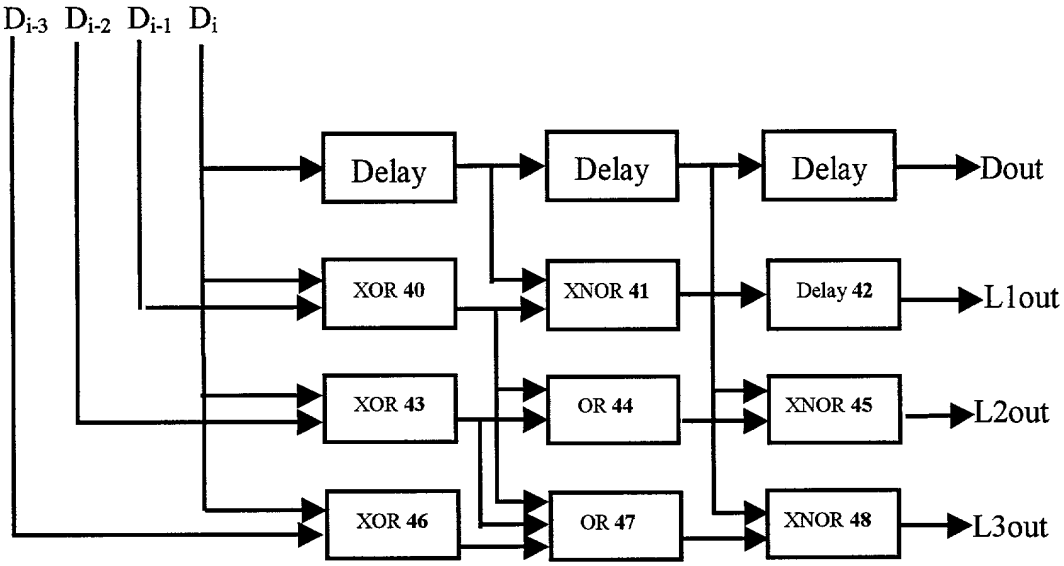

Fig. 6 A block diagram for the equalization logic that generates the three signals levels

Sample Input Stream = 01000111100 (a = MSB; b = first to right of MSB; k = LSB)
a = 0; b = 1; c = 0; d = 0; e = 0; f = 1; g = 1; h = 1; l = 1; j = 0; k = 0

Bit Identity	Dout	L1out	L2out	L3out
a	0	--------	----------	----------
b	1	1	1	1
c	0	0	0	0
d	0	**1**	0	0
e	0	**1**	**1**	0
f	1	1	1	1
g	1	**0**	1	1
h	1	**0**	**0**	1
l	1	**0**	**0**	**0**
j	0	0	0	0
k	0	**1**	0	0

Fig. 7

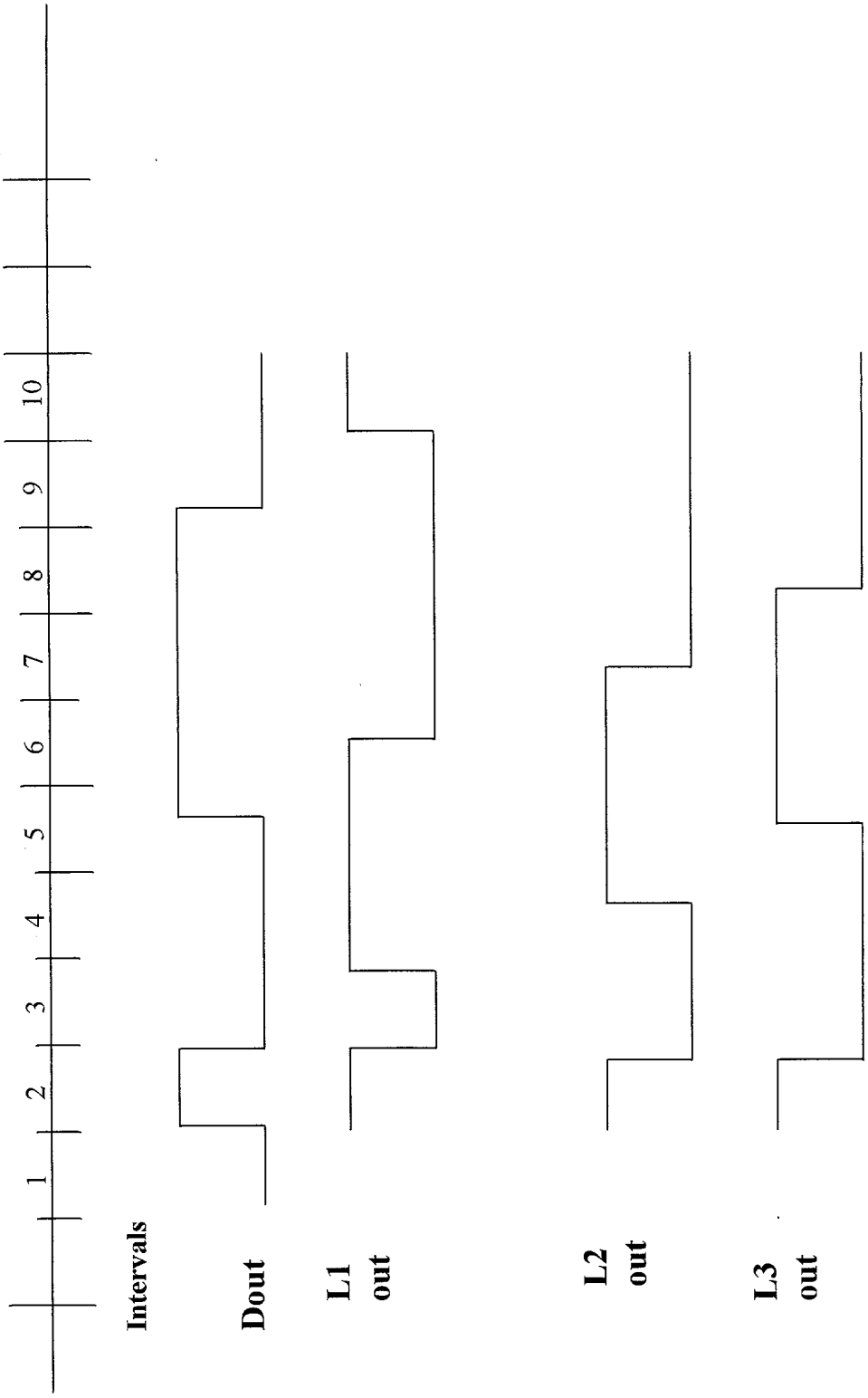

Fig. 8

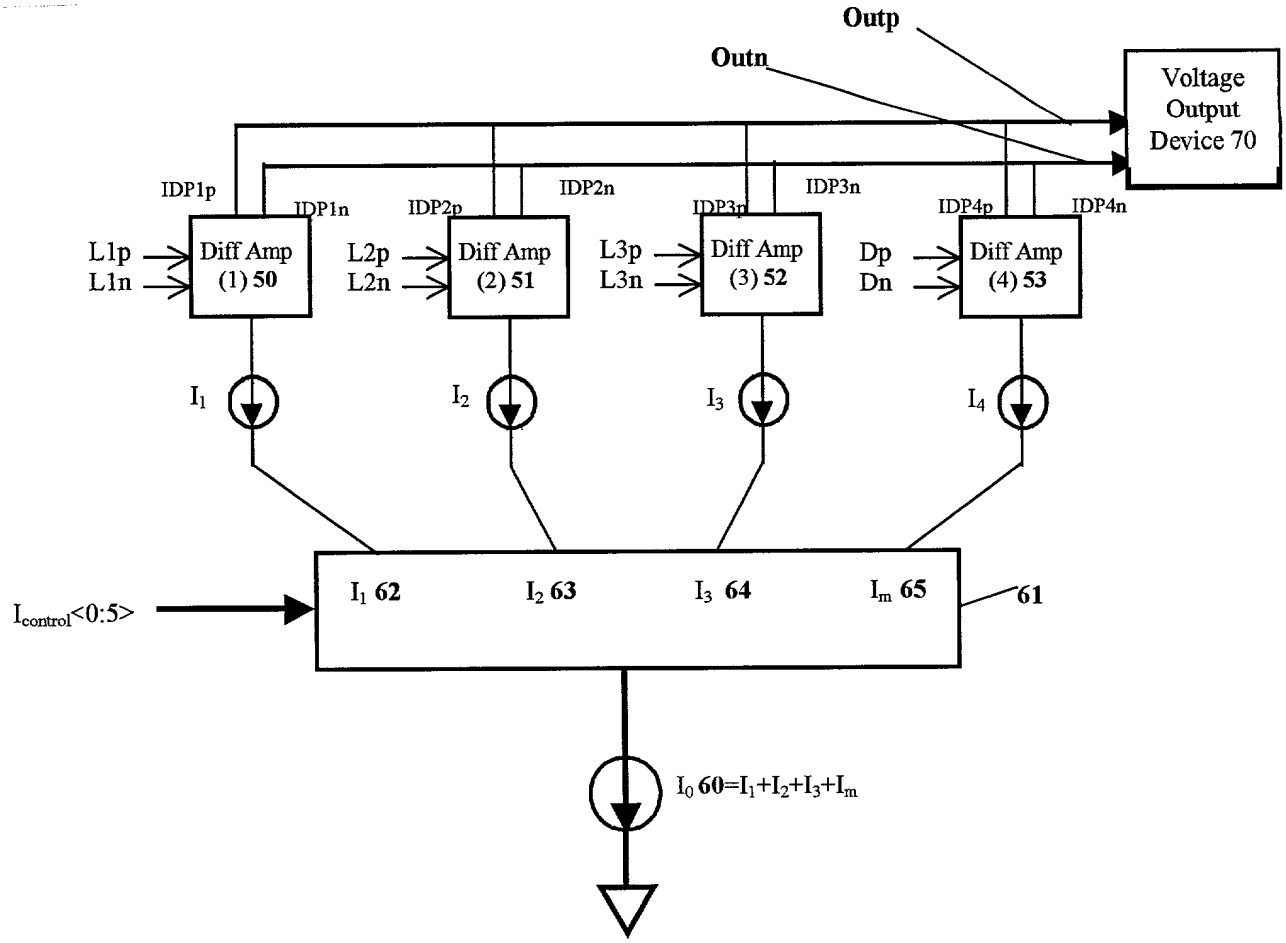
Outp
Outn
Voltage Output Device 70
IDP1p
IDP1n
IDP2p
IDP2n
IDP3p
IDP3n
IDP4p
IDP4n
L1p
L1n
Diff Amp (1) 50
L2p
L2n
Diff Amp (2) 51
L3p
L3n
Diff Amp (3) 52
Dp
Dn
Diff Amp (4) 53
I1
I2
I3
I4
Icontrol<0:5>
I1 62
I2 63
I3 64
Im 65
61
I0 60=I1+I2+I3+Im

Fig.9

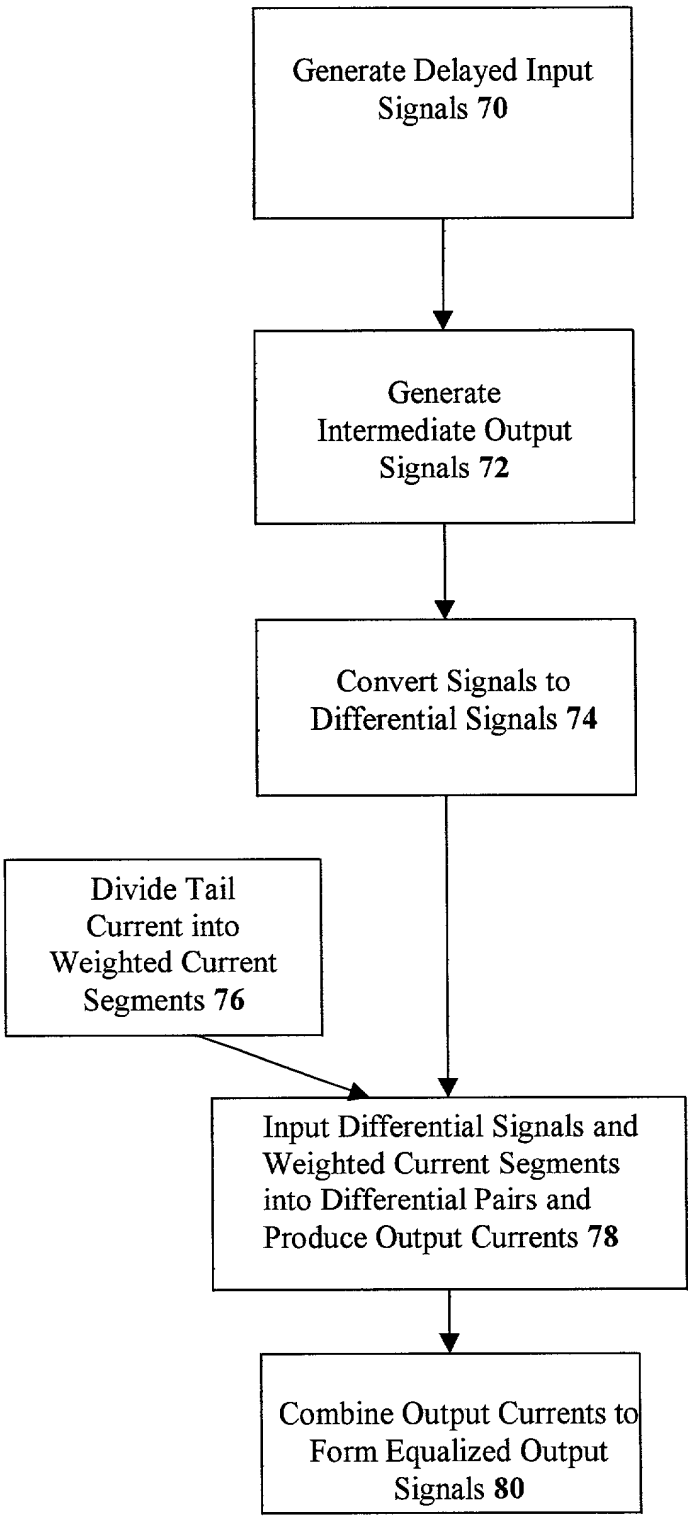
Generate Delayed Input Signals 70
Generate Intermediate Output Signals 72
Convert Signals to Differential Signals 74
Divide Tail Current into Weighted Current Segments 76
Input Differential Signals and Weighted Current Segments into Differential Pairs and Produce Output Currents 78
Combine Output Currents to Form Equalized Output Signals 80

Fig. 10